Clean Copy of Claims

The following is a clean copy of amended claims 1, 8 and 12.

1. An integrated circuit including an embedded memory and a built-in self-test arrangement including

means for storing test instructions including means for discriminating a source of a test command and receiving test instructions provided from an external tester,

means for generating default test instructions, and

means for supplying said default test instructions to said means for storing test instructions.

8. An electronic system including an integrated circuit having a built-in self-test arrangement therein, said integrated circuit including

means for storing test instructions including means for discriminating a source of a test command and receiving test instructions provided from an external tester,

means for generating default test instructions in absence of instructions from an external tester, and

means for supplying said default test instructions to said means for storing test instructions.

12. A method of performing system level tests on an electronic system including an integrated circuit having a built-in self-test (BIST) arrangement therein for performing manufacturing level and board level testing and including means for storing a test algorithm, said method comprising steps of

discriminating a source of a test command,

providing a system level test algorithm from said BIST arrangement in absence of instructions from an external tester,

transferring said system level test algorithm to said means for storing a test algorithm in said BIST arrangement, and

operating said BIST arrangement using said system level test algorithm.